REMARKS

Claims 1, 6-8 and 11-13 are pending in the present application. Claims 1, 7 and 12 have been amended.

Claim Rejections-35 U.S.C. 103

Claims 1, 6-8 and 11-13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Ishizuka et al. reference (U.S. Patent No. 6,617,801) in view of the Tsuji reference (U.S. Patent No. 6,545,652). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of driving a display panel of claim 1 includes in combination among other features "variably controlling respective constant current values for driving the respective data lines, wherein said variably controlling the constant current values is implemented by individually comparing a reference voltage with a voltage of each of the respective data lines as driven by the constant current values, using respective comparators each having a first input connected to the reference voltage and a second input connected to a respective one of the data lines, and wherein said variably controlling the constant current values is further implemented by supplying a constant current to the data lines by respective first transistors, and by supplying an adjustment current to the data lines by respective second transistors responsive to control signals output from the comparators". Applicant respectfully submits that the method of driving a display panel of claim 1 would not have been obvious in view of the prior art as relied

upon by the Examiner for at least the following reasons.

The Examiner has interpreted data comparators 34 in Fig. 2 of the Tsuji reference as meeting the comparing of claim 1. However, as described beginning in column 7, line 49 of the Tsuji reference, pixel data are clocked into, and stored in, respective memory circuits 32 responsive to a latch clock signal. The pixel level data is subsequently compared in data comparators 34 with the value output from counter 33. The output signal from data comparators 34 are input to constant current driver section 35, whereby the output signals from data comparators 34 control the flow of constant current output from constant current driver section 35 to each current line 6 for a driver pulse with interval corresponding to the pixel level data value.

Accordingly, comparators 34 in Fig. 2 of the Tsuji reference each have a first input connected to an output provided from counter 33, and a second input connected to a pixel level data output provided from a respective different one of **memory circuits (flip-flops) 32**. That is, each of comparators 34 in Fig. 2 of the Tsuji reference have respective inputs that are connected to an output of counter 33 and an output of memory circuits 32 within constant current control circuit section 3. Comparators 34 in Fig. 2 of the Tsuji reference are not connected to respective ones of current lines 6, as would be necessary to meet the features of claim 1.

The examiner has asserted in the Response to Arguments section on pages 7-8 of the current Office Action dated October 14, 2008, that comparators 34 in Fig. 2 of the Tsuji reference compare data stored in respective memories 32 that "**represents** a

voltage of each of the respective data lines". However, regardless of what the content of memories 32 in Fig. 2 of the Tsuji reference may "represent" as asserted by the Examiner, comparators 34 simply and clearly do not have second inputs that are physically connected to current lines 6, as would be necessary to meet the features of claim 1. In order to maintain this rejection, the Examiner has improperly disregarded these recited features of claim 1. Since it is clear that comparators 34 in Fig. 2 of the Tsuji reference do not each have "a first input connected to the reference voltage and a second input connected to a respective one of the data lines", comparators 34 do not individually compare a reference voltage with a voltage of each of the respective data lines as driven by constant current values, as would be necessary to meet the features of claim 1. The Tsuji reference as relied upon thus does not overcome the acknowledged deficiencies of the primarily relied upon Ishizuka et al. reference.

If this rejection is to be maintained, the Examiner is respectfully requested to clearly establish on the record how comparators 34 in Fig. 2 of the Tsuji reference may be interpreted as having inputs connected to current lines 6, as would be necessary to meet the features of claim 1.

With further regard to this rejection, the current value of each of the data lines is controlled by individually comparing a reference voltage with a voltage of each of the respective data lines using respective comparators. Thus, the current of each of the data lines are individually controlled. Moreover, variable control of the constant current values is further implemented by supplying constant currents to the data lines by

respective first transistors, and by supplying adjustment currents to the data lines by respective second transistors responsive to control signals.

In Fig. 3 of the primarily relied upon Ishizuka et al. reference, current from anode power source 10 is controlled responsive to a detected result as provided by anode voltage detection circuit 15. As shown, **one** anode voltage detection circuit 15 is connected to anode lead A_m. The Ishizuka et al. reference as relied upon by the Examiner therefore does not use respective variable control on each of respective data lines using respective comparators, as would be necessary to meet the features of claim 1. The circuit in Fig. 3 of the Ishizuka et al. reference is not capable of individually controlling a current of each of anode leads $A_1 - A_m$.

Moreover, the circuit in Fig. 3 of the Ishizuka et al. reference merely shows respective constant current drivers $2_1 - 2_m$. The Ishizuka et al. reference does not disclose or even remotely suggest variably controlling constant current values by supplying a constant current to data lines by respective first transistors, and by supplying an adjustment current to the data lines by respective second transistors responsive to control signals, as would be necessary to meet the features of claim 1.

In Fig. 2 of the secondarily relied upon Tsuji reference, as asserted previously, comparators 34 do not compare a reference voltage with a voltage of current lines 6. Comparators 34 clearly function in a different manner than as recited in claim 1. Moreover, constant current driver section 35 in Fig. 2 of the Tsuji reference is not disclosed or suggested as variably controlling constant current values by supplying a

constant current to data lines by respective first transistors, and by supplying an adjustment current to the data lines by respective second transistors responsive to control signals. The Tsuji reference as relied upon does not overcome the above noted deficiencies of the primarily relied upon Ishizuka et al. reference. Accordingly, Applicant respectfully submits that the method for driving a display panel of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1 and 6, is improper for at least these reasons, in addition to the reasons as set forth in the Amendment dated July 23, 2008.

The drive of a display panel of claim 7 includes in combination among other features comparison means "respectively provided for each of the data lines, said comparison means each having a first input coupled to a respective one of the data lines and for outputting a control signal by comparing a reference voltage from a reference voltage generator with a potential of the respective one of the data lines;... each of the variable current sources having a first transistor and a second transistor connected to the respective data lines, the first transistors supplying constant currents to the respective data lines and the second transistors supplying adjustment currents to the respective data lines responsive to the control signals". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

Comparators 34 in Fig. 2 of the Tsuji reference cannot be interpreted as the

comparison means of claim 7. As asserted previously, comparators 34 in Fig. 2 of the Tsuji reference each have a first input connected to a variable counter output provided by counter 33, and a second input coupled to pixel level data output from respective memory circuits 32. Comparators 34 in Fig. 2 of the Tsuji reference do not each have an input coupled to a respective one of the data lines, as would be necessary to meet the features of claim 7. Moreover, current sources are not specifically identified in Fig. 2 of the Tsuji reference. The Tsuji reference as relied upon does not include in Fig. 2 variable current sources that each have first transistors that supply constant currents to respective data lines, and second transistors that supply adjustment currents to respective data lines responsive to control signals. The Ishizuka et al. reference also does not disclose these features. Applicant therefore respectfully submits that the drive of a display panel of claim 7 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 7, 8 and 11, is improper for at least these reasons, in addition to the reasons as set forth in the Amendment dated July 23, 2008.

The drive of a display panel of claim 12 includes in combination among other features comparators "respectively provided for each of the data lines, the comparators each having a first input coupled to a respective one of the data lines, the comparators each output control signals by comparing a reference voltage from a voltage generator with a potential of the respective one of the data lines;... each of the variable current sources having a first transistor and a second transistor both connected to the

respective data lines, the first transistors supplying constant currents to the respective data lines, and the second transistors supplying adjustment currents to the respective data lines responsive to the control signals".

Applicant respectfully submits that the drive of a display panel of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 12 and 13, is improper for at least somewhat similar reasons as set forth above with respect to claim 7, and in further view of the reasons as set forth in the Amendment dated July 23, 2008.

Conclusion

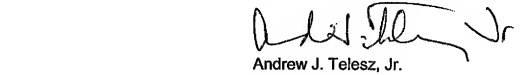
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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